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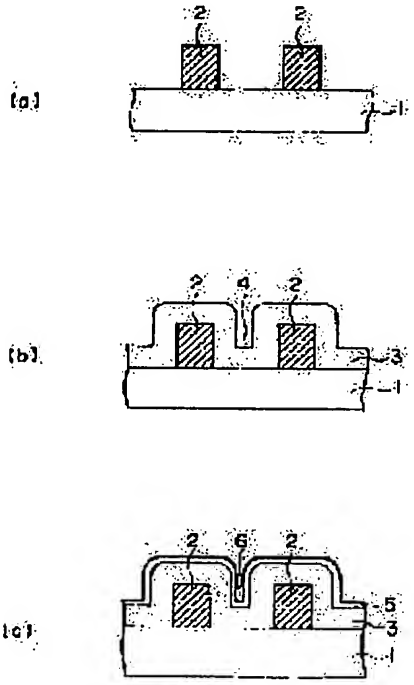
(54) METHOD FOR BASE SURFACE REFORMATION AND MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To eliminate influence of the surface dependability of a base layer surface, not depending on the condition of the base layer surface, by forming a base insulating film on a substrate, exposing the surface of the base insulating film to reform the surface prior to film formation.
SOLUTION: On the surface of a Si3N4 film 3, a Low O3/TEOS CVD SiO2 film 5 (base insulating film) is formed. After heating the film 5 to a temperature of 350°C at the surface, the surface of the film 5 is brought into contact with a plasma flow of ammonia (NH3) for 15 seconds to 5 minutes to reform the surface of the film 5. A High O3/TEOS CVD SiO2 film 7 is formed on the surface of the Low O3/TEOS CVD SiO2 film 5 by plasma CVD. Thus, influence of the surface dependability of a substrate is eliminated, not depending on the condition of the surface of the substrate.



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CLAIMS

[Claim(s)]
[Claim 1] The substrate surface treatment approach characterized by forming a substrate insulator layer on a substrate, and putting and carrying out surface treatment of the front face of this substrate insulator layer to plasma gas before membrane formation.
[Claim 2] Said substrate is the substrate surface treatment approach according to claim 1 characterized by having a crevice field.
[Claim 3] Said crevice field is the substrate surface treatment approach according to claim 2 characterized by being the slot formed in said substrate, or being a crevice between the wiring layers formed on the insulating layer.
[Claim 4] The substrate surface treatment approach according to claim 1 to 3 characterized by silicon oxide or a silicon nitride being exposed to the front face of said substrate.
[Claim 5] Said substrate insulator layer is the substrate surface treatment approach according to claim 1 to 4 characterized by being silicon oxide, the PSG film, the BSG film, or the BPSG film.
[Claim 6] Said silicon oxide is the substrate surface treatment approach according to claim 5 characterized by making tetraethyl orthochromatic silicate and ozone content gas react, and forming.
[Claim 7] Said ozone content gas is the substrate surface treatment approach according to claim 6 characterized by the ozone level in oxygen being 1% or less.
[Claim 8] Said silicon oxide is SiH2Cl2. N2O The substrate surface treatment approach according to claim 5 characterized by making it react and forming.
[Claim 9] Said silicon oxide is the substrate surface treatment approach according to claim 5 characterized by making tetraethyl orthochromatic silicate and oxygen react and forming.
[Claim 10] The thickness of said substrate insulator layer is the substrate surface treatment approach according to claim 1 to 9 characterized by being 100A or more.
[Claim 11] The substrate surface treatment approach according to claim 1 to 10 characterized by heating said substrate while having put the front face of said substrate insulator layer to plasma gas.

[Claim 12] The temperature of said substrate heating is the substrate surface treatment approach according to claim 11 characterized by being beyond a room temperature.
[Claim 13] The temperature of said substrate heating is the substrate surface treatment approach according to claim 12 characterized by being in the range of 100 degrees C or more and 400

degrees C or less.
[Claim 14] Said plasma gas is the substrate surface treatment approach according to claim 1 to 13 characterized by being generated using NH3, helium, Ar and O2, or the N2 O at least.
[Claim 15] The manufacture approach of the semiconductor device characterized by forming an insulator layer on said substrate insulator layer after performing reforming of a substrate insulator layer front face by the substrate surface treatment approach according to claim 1 to 14.
[Claim 16] Said insulator layer is the manufacture approach of the semiconductor device according to claim 15 characterized by being the silicon oxide which the ozone level in oxygen made the ozone content gas and tetraethyl orthochromatic silicate which are 4% or more react, and formed.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] reactant gas (it is hereafter described as O3 / TEOS reactant gas.) containing the ozone content gas by which especially this invention contains ozone (O3) in oxygen (O2) about the substrate surface treatment approach and the manufacture approach of a semiconductor device, and tetraethyl orthochromatic silicate (TEOS:Tetraethylorthosilicate) used CVD (Chemical Vapor Deposition) -- it is related with the substrate surface treatment approach before membrane formation by law, and the manufacture approach of a semiconductor device.
[0002]
[Description of the Prior Art] O3-/TEOS CVD using reactant gas Film which formed membranes by law (it is hereafter described as O3-/TEOS CVD SiO2 film.) Even if it is so precise that O3 concentration in O2 is high, and an etching rate is small and carries out elevated-temperature heat treatment, it does not contract, but there are few contents of moisture and what has a good flow property is obtained. Hereafter, high-concentration O3 is included. It is the thing of the silicon oxide which formed membranes using O3-/TEOS reactant gas (it is hereafter described as High O3/TEOS reactant gas.) High O3/TEOS CVD SiO2 It is described as the film and low-concentration O3 is included. The thing of the silicon oxide which formed membranes using O3-/TEOS reactant gas (it is hereafter described as Low O3/TEOS reactant gas.) is described as Low O3/TEOS CVD SiO2 film.
[0003] High O3/TEOS CVD SiO2 It depends for the film on the condition of the front face of a substrate layer greatly. especially -- SiO2 film -- or -- Front-faces top, such as Si3N4 film If High O3/TEOS CVD SiO2 film is formed, abnormality growth will arise, and as shown in drawing 11 , the fall of membranous porous-izing, the surface dry area of a membranous front face, and a membrane formation rate is produced. On the other hand, when Low O3/TEOS CVD SiO2 film was formed on the front face of a substrate layer, it mentioned above on this Low O3/TEOS CVD SiO2 film. Abnormality growth like High O3/TEOS CVD SiO2 film is not seen. However, compared with Low

O3/TEOS CVD SiO2 film and High O3/TEOS CVD SiO2 film, membraneous qualities, such as compactness, are inferior.
[0004] Therefore, it is made not to receive effect in the surface state of a substrate layer. In order to obtain smooth film formation, film formation of high quality, and the good pad nature to a narrow crevice field, it is necessary to form High O3/TEOS CVD SiO2 film. There are the following approaches among the approaches for eliminating the surface dependency of a substrate layer before membrane formation of High O3/TEOS CVD SiO2 film conventionally.
[0005] (1) as [show / as shown / 1st / in drawing 12 (a) / approach of irradiating plasma is shown in front face of substrate layer 120, and / at drawing 12 (b) / on the substrate layer 120 by which reforming was carried out] -- form High O3/TEOS CVD SiO2 film 121.
(2) it is shown [2nd] in drawing 13 (a) -- as -- the substrate layer 130 -- covering -- plasma CVD as [show / there is approach of forming plasma SiO2 film 131 of substrate insulator layer by law, and / at drawing 13 (b) / on substrate insulator layer 131] -- High O3/TEOS CVD SiO2 film 132 is formed.
[0006] Plasma CVD at the time of forming plasma SiO2 film 131 The conditions of membrane formation by law are accepted and it is High O3/TEOS CVD SiO2. The film 132 and plasma SiO2 film 131 with sufficient membrane formation top compatibility can be obtained. Therefore, after forming plasma SiO2 film 131 with this sufficient compatibility as a substrate insulator layer on the front face of the substrate layer 130, it is High O3/TEOS CVD SiO2 on plasma SiO2 film 131 front face. High O3/TEOS CVD SiO2 which had the outstanding membraneous quality when forming the film 132 The film can be obtained.
[0007] (3) O3/TEOS CVD SiO2 film (it is hereafter described as low voltage O3/TEOS CVD SiO2 film.) which covered the front face of the substrate layer 140 and was formed [3rd] under Low O3/TEOS CVD SiO2 film 141 of a substrate insulator layer, or low voltage as shown in drawing 14 (a) -- there is the approach of forming 141 and it is shown on the substrate insulator layer 141 at drawing 14 (b) -- as -- High O3/TEOS CVD SiO2 The film 142 is formed. HighO3/TEOS CVD SiO2 film 142 is good, and since the membrane formation rate on it is quick, Low O3/TEOS CVDSiO2 film or low voltage O3-/TEOS CVD SiO2 film 141, and compatibility tend to form it.
[0008]
[Problem(s) to be Solved by the Invention] However, there are the respectively following problems by the conventional approach mentioned above. That is, by the approach of carrying out the plasma exposure of the front face of (1) substrate layer 120, neither according to the class of substrate layer 120 front face, nor the conditions of a plasma exposure, the surface dependency of the substrate layer 120 may be able to be eliminated, or may be made. Therefore, the conditions of a plasma exposure do not say that it can communalize and standardize about all the substrate layer 120, and needed to be optimized each time according to the condition of the substrate layer 120.
[0009] (2) By the approach of forming plasma SiO2 film 131 as a substrate insulator layer, plasma SiO2 film 131 has a bad step hippo ridge, and it is not fit for application in the existing detailed and substrates layer, such as a trench.
(3) By the approach of forming Low O3/TEOS CVD SiO2 film 141 or low voltage O3-/TEOS CVD SiO2 film 141 as a substrate insulator layer before membrane formation of High O3/TEOS CVD SiO2 film 142, Low O3/TEOS CVD SiO2 film etc. has an isotropic film formation property, and further, 141 needs the thickness of 1000A or more as thickness, in order to make it not influenced of the surface dependency of the substrate layer 130. Therefore, it is not fit for detailed and application in existing substrate layers, such as a trench. Moreover, compared with 141 and High O3/TEOS CVD SiO2 film, such as Low O3/TEOS CVD SiO2 film, compactness is low and unsuitable as a substrate insulator layer.
[0010] This invention is created in view of the trouble of the starting conventional example, and moreover, it aims at detailed and offering the substrate surface treatment approach which can apply a trench etc. also to the substrate layer which it has (for example, between a trench slot and a

metal wiring layer, between metal lower layers, etc.), and the manufacture approach of a semiconductor device, without being influenced of the surface dependency of a substrate layer front face, without being based on the condition of a substrate layer front face.
[0011]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, this invention relates to the substrate surface treatment approach, a substrate insulator layer is formed on a substrate before membrane formation, and it is characterized by putting and carrying out surface treatment of the front face of this substrate insulator layer to plasma gas. Said substrate is characterized by having a crevice between a crevice field, for example, the slot formed in the substrate, and the wiring layer formed on the insulating layer.
[0012] Moreover, said silicon oxide makes tetraethyl orthochromatic silicate and ozone content gas react, and is formed, and ozone content gas is characterized by the ozone level in oxygen being 1% or less. Moreover, thickness of said substrate insulator layer is characterized by being 100A or more. Moreover, said plasma gas is characterized by being generated using NH3, helium, Ar and O2, or the N2O at least.
[0013] Moreover, in order to solve the above-mentioned technical problem, after this invention's relating to the manufacture approach of a semiconductor device and performing reforming of a substrate insulator layer front face by the above-mentioned substrate surface treatment approach, it is characterized by forming an insulator layer on said substrate insulator layer. Said insulator layer is characterized by being the silicon oxide which the ozone level in oxygen made the ozone content gas and tetraethyl orthochromatic silicate which are 4% or more react, and formed.
[0014] According to the substrate surface treatment approach of this invention, before membrane formation, a substrate insulator layer is formed on a substrate and the plasma exposure of the front face of a substrate insulator layer is carried out further. Since the substrate insulator layer is formed on a substrate before membrane formation, the effect of the surface dependency of a substrate can be avoided without being based on the condition on the front face of a substrate. Furthermore, since the plasma exposure of the front face of a substrate insulator layer is carried out, the front face of a substrate insulator layer can be reformed. In this case, since what is necessary is just to reform the front face of the substrate insulator layer formed in the substrate front face instead of the front face itself of a substrate considered to have a different surface state for every form, the surface treatment approach communalized and standardized can be acquired.
[0015] Since reforming of the front face of a substrate insulator layer is carried out by this when forming membranes on a substrate insulator layer, an insulator layer etc. can be formed on a substrate insulator layer, without being influenced of a substrate surface dependency. Moreover, according to the experiment of an invention-in-this-application person, it turned out that thickness of the substrate insulator layer which will not receive the effect of the surface dependency of a substrate in a substrate insulator layer if a plasma exposure is carried out can be made thinner.
[0016] For example, O2 Inner O3 When concentration formed a substrate insulator layer using 1% or less of ozone content gas, and tetraethyl orthochromatic silicate (TEOS) gas, the 100A of the minimum thickness which stops influencing of the surface dependency of a substrate was obtained. According to this invention, since the plasma exposure of the front face of a substrate insulator layer is carried out, the membraneous quality of a substrate insulator layer becomes precise, and even if it makes thickness of a substrate insulator layer thin, effect of the surface dependency of a substrate can be influenced and carried out.
[0017] Moreover, since thickness of a substrate insulator layer can be made thin, according to an invention-in-this-application person's experimental result, formation of the substrate insulator layer to the substrate which has a crevice field with a very narrow width of face [between a trench slot and a metal wiring layer, between metal lower layers, etc.] of about 0.1 micrometers is attained. When a substrate insulator layer was formed on the substrate front face which has the crevice field of very narrow width of face using the ozone content gas and TEOS which contain low

concentration ozone especially, it turned out that surface smoothness, step hippo ridge nature, and embedding nature are excellent, and a substrate insulator layer with high compactness is moreover obtained.

[0018] Furthermore, according to the manufacture approach of the semiconductor device of this invention, before membrane formation of an insulator layer, after forming a substrate insulator layer on a substrate, a substrate insulator layer front face is reformed by plasma exposure, and the insulator layer is formed on it. For this reason, the good insulator layer of membraneous quality can be formed, without [minutely and] being able to apply also to the substrate which has a trench etc. (for example, between a trench slot and a metal wiring layer, between metal lower layers, etc.), and being influenced of the surface dependency of a substrate.

[0019] When a substrate insulator layer is formed using the ozone content gas and TEOS which contain 1% or less of low concentration ozone especially and an insulator layer is formed using the ozone content gas and TEOS containing 4% or more of high concentration ozone on the substrate insulator layer by which reforming was carried out, the compatibility on membrane formation with a substrate insulator layer and an insulator layer is very good, and is a desirable combination.

[0020]

[Embodiment of the Invention] Hereafter, the substrate surface treatment approach before membrane formation concerning the gestalt of operation of this invention and the manufacture approach of a semiconductor device are explained, referring to a drawing. After forming Low O3/TEOS CVD SiO2 film 5 on a silicon wafer 1 with the gestalt of this operation, it is the front face of Low O3/TEOS CVD SiO2 film 5 NH3 It puts into the plasma, the front face of Low O3/TEOS CVD SiO2 film 5 is reformed, and it is High O3/TEOS CVD SiO2 on the front face of after that and Low O3/TEOS CVD SiO2 film 5. The film 7 is formed.

[0021] The equipment used for the plasma exposure to the front face of Low O3/TEOS CVD SiO2 film 5 is plasma equipment of the parallel monotonous mold of the anode plate coupling scheme shown in drawing 9 . In the chamber 91 of this equipment, the up electrode RF 92 and the lower electrode LF 93 are countered and installed, RF generator 94 with a frequency of 13.56MHz is connected to the up electrode RF 92, and the 380kHz low frequency power source 95 is connected to the lower electrode LF 93. The gas installation piping 96 is connected to the chamber 91, and it is NH3 from this gas installation piping 96. Gas is introduced in a chamber 91.

[0022] Next, how to perform substrate surface treatment processing using the above-mentioned surface treatment processor is explained. Drawing 1 is the sectional view showing the manufacture approach of a semiconductor device of having used the substrate surface treatment approach of the gestalt operation of this invention. First, patterning is carried out and wiring 2 is formed, after forming the polish recon film on a silicon wafer 1, as shown in drawing 1 (a). At this time, spacing during the adjoining wiring 2 carries out patterning so that it may be set to 0.5 micrometers.

[0023] Next, as shown in drawing 1 (b), the silicon nitride (Si3N4 film) 3 of 200nm of thickness is formed so that a silicon wafer 1 and wiring 2 may be covered. Si3N4 whose width of face is 0.1 micrometers between the adjoining wiring 2 at this time and whose depth is 0.5 micrometers The slot (crevice) 4 covered with the film 3 is formed. The above constitutes a substrate. And after heating so that the temperature of the front face of Si3N4 film 3 may become 400 degrees C, it puts to the ozone content gas containing low-concentration O3 whose concentration in O2 is 1% or less about the front face of Si3N4 film 3, and the mixed gas (Low O3/TEOS reactant gas is called hereafter.) of TEOS.

[0024] Low O3/TEOS CVD SiO2 film 5 (substrate insulator layer) is formed on the front face of the like and Si3N4 film 3 which are shown after predetermined time at drawing 1 (c). At this time, Low O3/TEOS CVD SiO2 film 5 is formed so that thickness may become 100A or more. Thickness of Low O3/TEOS CVD SiO2 film 5 is made thin with 100A for covering the inside of the slot 4 of narrow width of face, without reducing the step coverage nature to the slot 4 of narrow width of face. Moreover, let 100A be a minimum for not being influenced of the surface dependency of a

substrate.
[0025] Moreover, Si3N4 Since Low O3/TEOS CVD SiO2 film 5 is formed in the slot 4 covered with the film 3, width of face is set to 0.08 micrometers, and, as for the slot 6 covered with Low O3/TEOS CVD SiO2 film 5, the depth is set to 0.49 micrometers. after [furthermore,] heating so that the temperature of the front face of Low O3/TEOS CVD SiO2 film 5 may become 350 degrees C as shown in drawing 2 (a) -- the front face of Low O3/TEOS CVD SiO2 film 5 -- the plasma style of ammonia (NH3) -- 15 seconds thru/or a 5-minute about room -- it is made to contact and surface treatment processing of the front face of Low O3/TEOS CVD SiO2 film 5 is performed.
[0026] Since what is necessary is to reform only the front face of Low O3/TEOS CVD SiO2 film 5, without being involved in the class of substrate since the front face of Si3N4 film 3 is covered with Low O3/TEOS CVD SiO2 film 5 this time, substrate surface treatment conditions can be communalized and it can standardize. Moreover, eburnation of the Low O3/TEOS CVD SiO2 film 5 is carried out by reforming, and it is High O3/TEOS CVDSiO2. It can consider as membraneous quality equivalent to the film. For this reason, in spite of making thin thickness of Low O3/TEOS CVD SiO2 film 5 to 100A, it can avoid being influenced of the surface dependency of Si3N4 film 3. Therefore, the surface treatment of a substrate which has a detail, a trench, etc. also becomes possible.
[0027] Next, after heating so that the temperature of the front face of Low O3/TEOS CVD SiO2 film 5 may become 400 degrees C as shown in drawing 2 (b) Mixed gas of the ozone content gas and TEOS in which the concentration in O2 contains 4% or more of high-concentration O3 (the following and High O3/TEOS reactant gas are called.) By the used plasma-CVD method, it is on the front face of Low O3/TEOS CVD SiO2 film 5. High O3/TEOS CVD SiO2 film 7 is formed. This time, High O3/TEOS CVD SiO2 film 7 will fill the inside of a slot 6 completely, and will cover Low O3/TEOS CVD SiO2 film 5 completely further.
[0028] The front face of Si3N4 film 3 is covered with Low O3/TEOS CVD SiO2 film 5. It is made not to be influenced of the surface dependency of Si3N4 film 3, and the front face of Low O3/TEOS CVD SiO2 film 5 is reformed. For this reason, it is on Low O3/TEOS CVD SiO2 film 5, without producing abnormality growth. High O3/TEOS CVD SiO2 film 7 can be formed. Next, the experiment which the invention-in-this-application person conducted is explained below. It investigated about the following three items.
[0029] High O3/TEOS CVD SiO2 [as opposed to the thickness of Low O3/TEOS CVD SiO2 film 5 to the 1st] The membrane formation velocity ratio of the film 7 was investigated, and the relation between the thickness of Low O3/TEOS CVD SiO2 film 5 and a surface dependency was investigated. HighO3/TEOS CVD SiO2 [as opposed to the plasma irradiation time to the front face of Low O3/TEOS CVD SiO2 film 5 to the 2nd] The membrane formation velocity ratio of the film 7, and High O3/TEOS CVD SiO2 It investigated about the substrate surface dependency at the time of forming the film 7.
[0030] High O3/TEOS CVD SiO2 which formed membranes to the 3rd It investigated also about the surface smoothness, step hippo ridge nature, and embedding nature of the film 7. The detailed contents and the result of the above-mentioned experiment are explained below. Forming Low O3/TEOS CVD SiO2 film 5 as a substrate insulator layer on a silicon nitride, the plasma exposure to the front face of Low O3/TEOS CVD SiO2 film 5 is NH3. It carried out for 2 minutes using the plasma style.
[0031] Drawing 3 is High O3/TEOS CVD SiO2 to the thickness of Low O3/TEOS CVD SiO2 film 5. It is the graph which shows the membrane formation velocity ratio of the film 7. The thickness of Low O3/TEOS CVD SiO2 film 5 was taken along the axis of abscissa, and the membrane formation velocity ratio was taken along the axis of ordinate. A membrane formation velocity ratio is High O3/TEOS CVD SiO2 directly on a silicon wafer 1. It is High O3/TEOS CVD SiO2 on Low O3/TEOSCVD SiO2 film 5 to the membrane formation rate when forming the film 7. The ratio of the membrane formation rate when forming the film 7 is expressed.

[0032] If there is 100A or more of thickness of Low O3/TEOS CVD SiO2 film 5 from the result shown in drawing 3 , it will be High O3/TEOS CVD SiO2. Although a change is almost lost with the time of the membrane formation rate of the film 7 forming membranes on a silicon wafer 1 If it is 100A or less of thickness, when a membrane formation rate becomes slow gradually and 0A is approached so that thickness becomes thin, it turns out that about 80% of the membrane formation rate when forming membranes on a silicon wafer 1 is approached.
[0033] Therefore, it can be made extent same if there is 100A or more as the time of forming a membrane formation rate on a silicon wafer 1, and the thickness of Low O3/TEOS CVD SiO2 film 5 is High O3/TEOS CVD SiO2. It turns out that the substrate surface dependency at the time of forming the film 7 is eliminable. Drawing 4 is a graph which shows the membrane formation velocity ratio to plasma irradiation time. The plasma irradiation time of the front face of Low O3/TEOS CVD SiO2 film 5 is taken along an axis of abscissa, and it is High O3/TEOSCVD SiO2 to an axis of ordinate. The membrane formation velocity ratio of the film 7 was taken. A membrane formation velocity ratio means the same thing as drawing 3 .
[0034] In this case, thickness of Low O3/TEOS CVD SiO2 film 5 was set constant 100A. For the plasma irradiation time to Low O3/TEOS CVD SiO2 film 5, from drawing 4 , a membrane formation rate is High O3/TEOS CVD SiO2 directly on a silicon wafer 1 at about 1 or less minute. It turned out that it becomes earlier than the membrane formation rate when forming the film 7, and the effect of a substrate dependency can be removed completely. Moreover, even if it acts as the merit of the plasma irradiation time 1 minute or more, a membrane formation rate does not become slow quickly and it is thought that it can fully be equal to practical use. Thus, it turned out about plasma irradiation time that the margin to the improvement effect of a substrate dependency is large.
[0035] Drawing 10 (a) and (b) formed membranes according to the manufacture approach and manufacture conditions concerning this example. It is the photograph in which the cross-section configuration and surface state of High O3/TEOS CVD SiO2 film 7 are shown. Membranes were formed as shown in drawing 10 (a) and (b). It turns out that High O3/TEOS CVD SiO2 film 7 is excellent in surface smoothness, step hippo ridge nature, and embedding nature. In addition, although Low O3/TEOS CVD SiO2 film 5 is used with the gestalt of this operation Instead PSG () [Phosphosilicate] the glass film and BSG (Borophophosilicate glass) The film and BPSG (Borophophosilicate glass) The film, low voltage O3-/TEOS SiO2 film, SiH2Cl2, and N2O Either SiH2Cl2/N2O SiO2 film which is made to react and is formed or the O2/TEOS SiO2 film which O2 and TEOS are made to react and are formed may be used.
[0036] PSG As gas for membrane formation in the case of forming the film, they are O3, TEOS, and TMP (Trimetylphosphite:P (OCH3)3.). Or mixed gas with TMOP (Trimethylphosphate:PO3 (OCH3)) is used. BSG As gas for membrane formation in the case of forming the BPSG film, using the mixed gas of O3, TEOS, and TMB (Trimetylborate:B3 (OCH3)) as gas for membrane formation in the case of forming the film O3, TEOS, and TMB TMP Or mixed gas with TMOP can be used.
[0037] PSG The film and BSG The time of forming the film, the BPSG film, or the low voltage O3-/TEOS SiO2 film, it heats so that the front face of Si3N4 film 3 may become 350 degrees C or more. Moreover, when forming either SiH2Cl2/N2O SiO2 film or the O2/TEOS SiO2 film, it heats so that the front face of Si3N4 film 3 may become 650 degrees C or more. While carrying out the plasma exposure on the front face of Low O3/TEOS CVD SiO2 film 5, whenever [stoving temperature / of the front face of Low O3/TEOS CVD SiO2 film 5] should just be 100 degrees C - 400 degrees C more preferably that what is necessary is just beyond a room temperature.
[0038] Furthermore, although temperature of the front face of Low O3/TEOS CVD SiO2 film 5 is made into 400 degrees C at the time of membrane formation of High O3/TEOS CVD SiO2 film 7, what is necessary is just 350 degrees C or more in temperature. Moreover, the gas used for plasma treatment is NH3. Although the biggest effectiveness can be acquired about surface treatment, Ar, helium, N2O, N2, and O2 grade may be used instead of NH3.
(The 1st example) Drawing 5 is the sectional view showing the substrate surface treatment

approach of this invention concerning the 1st example of this invention.
[0039] In this example, the trench slot (crevice) 52 whose width of face is 0.1 micrometers is formed in a silicon wafer 51, subsequently this trench slot 52 is covered and a substrate insulator layer is formed. And it investigated about the surface smoothness, step hippo ridge nature, and embedding nature of a substrate insulator layer. First, after forming the silicon oxide (SiO2 film) 53 of thin thickness on a silicon wafer 51, it is Si3N4 on SiO2 film 53. The film 54 is formed.
[0040] Subsequently, Si3N4 which should form a trench by patterning The film 54 and SiO2 film 53 are removed covering width of face of 150nm. Subsequently, Si3N4 which carried out patterning The film 54 and SiO2 film 53 are used as a mask, a silicon wafer 51 is etched, and the trench slot 52 whose width of face is 150nm is formed.
[0041] Next, SiO2 film 53 is formed in silicon wafer 51 front face exposed in the trench slot 52 by thermal oxidation, and it ties with SiO2 film 53 for a flat part. The above constitutes a substrate. Subsequently, the SiO2 film 53 top and Si3N4 After forming Low O3/TEOS CVD SiO2 film 55 by 10nm of thickness on the film 54 at homogeneity, it is the front face of Low O3/TEOS CVD SiO2 film 55 NH3 It puts to the plasma and the front face of Low O3/TEOS CVD SiO2 film 55 is reformed.
[0042] Next, it is High O3/TEOS CVD SiO2 on the front face of Low O3/TEOS CVD SiO2 film 55. The film 56 is formed. Since a substrate front face is covered and Low O3/TEOS CVD SiO2 film 55 is formed, it stops that a different ingredient is exposed to a substrate front face according to this experiment, but it can be prevented from being influenced of the surface dependency by ingredients differing.
[0043] Moreover, since the plasma exposure is carried out at Low O3/TEOS CVD SiO2 film 55, thickness of Low O3/TEOS CVD SiO2 film 55 can be made thin, and, thereby, the membrane formation to the narrow crevice field of trench slot 52 grade 100nm or less is attained. Moreover, since Low O3/TEOS CVD SiO2 film 55 is used, the surface smoothness, step hippo ridge nature, and embedding nature of a substrate insulator layer are excellent.
[0044] Therefore, it becomes possible to apply this invention to the substrate which has narrow crevice fields, such as a detail and a trench.
(The 2nd example) Drawing 6 is the sectional view showing the substrate surface treatment approach concerning this example, and the manufacture approach of the semiconductor device using it. This invention is applied to the substrate which consists of plasma SiO2 film which covers with this example the wiring layer formed on the insulator layer on a silicon wafer 61, and this wiring layer.
[0045] first, the SiOafter forming SiO2 film 62 on silicon wafer 612 film 62 top -- aluminum and TiN from -- the becoming wiring 63 is formed. Subsequently, wiring 63 is covered and plasma SiO2 film 64 of 0.1 micrometers of thickness is formed. Plasma SiO2 film 64 carries out the duty of wiring protection to moisture. Next, Low O3/TEOS CVD SiO2 film 65 of 0.05 micrometers of thickness is formed on plasma SiO2 film 64 in the slot 66 made along with the adjoining wiring 63, and plasma SiO2 film 64. At this time, since Low O3/TEOS CVD SiO2 film 65 has good compatibility with a substrate, Low O3/TEOS CVD SiO2 film 65 of uniform thickness is formed over the whole.
[0046] Subsequently, it is the front face of Low O3/TEOS CVD SiO2 film 65 NH3 It puts into the plasma and the front face of Low O3/TEOS CVD SiO2 film 65 is reformed. Then, it is High O3/TEOS CVD SiO2 to the front face of Low O3/TEOS CVD SiO2 film 65 of slot 66 inside and outside. The film 67 is formed. According to this experiment, since thickness of Low O3/TEOS CVD SiO2 film 65 is made thin, the membrane formation to the narrow crevice field between the wiring layers covered with plasma SiO2 film is possible.
[0047] Moreover, since Low O3/TEOS CVD SiO2 film 65 is used, Low O3/TEOS CVD SiO2 film 65 which formed membranes to the crevice field is excellent in surface smoothness, step hippo ridge nature, and embedding nature. Therefore, it becomes possible to apply this invention to the substrate which has narrow crevice fields, such as a detail and a trench.

(The 3rd example) Drawing 7 is the sectional view showing the substrate surface treatment approach concerning this example, and the manufacture approach of the semiconductor device using it. In this example, this invention is applied to the substrate which consists of an insulator layer of a semi-conductor substrate, and wiring which maintained narrow spacing, and was adjoined and formed on this. And wiring is covered and a substrate insulator layer is formed so that wiring may be touched directly. That is, the ingredient with which an insulator layer differs from the electric conduction film forms a direct substrate insulator layer on the substrate exposed to a front face.

[0048] first, a silicon wafer 71 top -- SiO2 film 72 -- forming -- further -- the SiO2 film 72 top -- aluminum and TiN from -- the becoming wiring 73 is formed. These wiring 73 is formed so that spacing during the adjoining wiring 73 may be set to 250nm. The above constitutes a substrate. Next, Low O3/TEOS CVD SiO2 film 75 of 20nm of thickness which covers wiring 73 is formed on SiO2 film 72. At this time, since Low O3/TEOS CVD SiO2 film 75 cannot be influenced not much easily of a substrate dependency, LowO3/TEOS CVD SiO2 film 75 of uniform thickness is formed over the inside and outside of slot 74 during wiring 73.

[0049] Subsequently, it is the front face of Low O3/TEOS CVD SiO2 film 75 NH3 It is High O3/TEOS CVD SiO2 on the front face of Low O3/TEOS CVD SiO2 film 75 of slot 74 inside and outside after putting to the plasma and reforming the front face of Low O3/TEOS CVD SiO2 film 75. The film 76 is formed. Since a different ingredient has covered with Low O3/TEOSCVD SiO2 film 75 the substrate front face exposed to a front face according to this experiment, the surface dependency by a different ingredient being exposed can be controlled. Thereby, it is High O3/TEOS CVD SiO2, without being influenced of a surface dependency on Low O3/TEOS CVD SiO2 film 75. The film 76 can be formed.

[0050] Moreover, since thickness of Low O3/TEOS CVD SiO2 film 75 is made thin, the membrane formation to the narrow crevice field between wiring layers is possible. Furthermore, Low O3/TEOS CVD SiO2 film 75 which formed membranes to the crevice field is excellent in surface smoothness, step hippo ridge nature, and embedding nature. Therefore, it becomes possible to apply this invention to reforming on the front face of a substrate which has narrow crevice fields, such as a detail and a trench.

(The 4th example) Drawing 8 is the sectional view showing the substrate surface treatment approach concerning this example. Wiring which equipped the flank of wiring with the sidewall spacer is covered with this example, and the substrate insulator layer is formed. The level difference at the time of covering a substrate insulator layer with a sidewall spacer is eased.

[0051] first, the SiOafter forming SiO2 film 82 on silicon wafer 812 film 82 top -- aluminum and TiN from -- the becoming wiring 83 is formed. This wiring 83 is formed so that spacing during the adjoining wiring 83 may be set to 100nm. Subsequently, after covering wiring 83 and forming SiO2 (or Si3N4) film, the sidewall spacer 84 is formed in the both-sides side of wiring 83 by anisotropic etching. Thereby, the side face of wiring 83 serves as a configuration of a skirt flare, and eases a level difference. A slot is formed between the sidewall spacers 84. The above constitutes a substrate.

[0052] Next, wiring 83 is covered and Low O3/TEOS CVD SiO2 film 85 of 10nm of thickness is formed. At this time, Low O3/TEOS CVD SiO2 film 85 of uniform thickness is formed within and without a slot. Subsequently, it is the front face of Low O3/TEOS CVD SiO2 film 85 NH3 It puts into the plasma and the front face of Low O3/TEOS CVD SiO2 film 85 is reformed.

[0053] Next, it is High O3/TEOS CVD SiO2 on the front face of Low O3/TEOS CVD SiO2 internal and external film 85 of a slot 86. The film 87 is formed. From this result, since a different ingredient has covered with Low O3/TEOS CVDSiO2 film 85 the substrate front face exposed to a front face, the surface dependency by a different ingredient being exposed can be controlled. Thereby, it is High O3/TEOS CVD SiO2, without being influenced of a surface dependency on Low O3/TEOS CVD SiO2 film 85. The film 86 can be formed. Moreover, since thickness of Low O3/TEOS CVD

SiO2 film 85 is made thin, the membrane formation to the narrow crevice field between wiring layers is possible. Furthermore, Low O3/TEOS CVD SiO2 film 85 which formed membranes to the crevice field is excellent in surface smoothness, step hippo ridge nature, and embedding nature. Therefore, it becomes possible to apply this invention to reforming on the front face of a substrate which has narrow crevice fields, such as a detail and a trench.

[0054]

[Effect of the Invention] As mentioned above, according to the substrate surface treatment approach of this invention, before membrane formation, a substrate insulator layer is formed on a substrate and the plasma exposure of the front face of a substrate insulator layer is carried out further. Since the substrate insulator layer is formed on a substrate before membrane formation, the effect of the surface dependency of a substrate can be avoided without being based on the condition on the front face of a substrate.

[0055] Furthermore, since the plasma exposure of the front face of a substrate insulator layer is carried out, the front face of a substrate insulator layer can be reformed. In this case, since what is necessary is just to reform the front face of the substrate insulator layer formed in the substrate front face instead of the front face itself of a substrate, the surface treatment approach communalized and standardized can be acquired. Since reforming of the front face of a substrate insulator layer is carried out by this when forming membranes on a substrate insulator layer, an insulator layer etc. can be formed on a substrate insulator layer, without being influenced of a substrate surface dependency.

[0056] Moreover, since the plasma exposure of the front face of a substrate insulator layer is carried out, the membraneous quality of a substrate insulator layer becomes precise, and even if it makes thickness of a substrate insulator layer thin, effect of the surface dependency of a substrate can be influenced and carried out. Therefore, formation of the substrate insulator layer to the substrate which has the crevice field of very narrow width of face is attained. When a substrate insulator layer is formed on the substrate front face which has the crevice field of very narrow width of face using the ozone content gas and TEOS which contain low concentration ozone especially, surface smoothness, step hippo ridge nature, and embedding nature are excellent, and, moreover, a substrate insulator layer with high compactness is obtained.

[0057] Furthermore, according to the manufacture approach of the semiconductor device of this invention, before membrane formation of an insulator layer, after forming a substrate insulator layer on a substrate, a substrate insulator layer front face is reformed by plasma exposure, and the insulator layer is formed on it. For this reason, the good insulator layer of membraneous quality can be formed, without [minutely and] being able to apply also to the substrate which has a trench etc. and being influenced of the surface dependency of a substrate. When a substrate insulator layer is formed using the ozone content gas and TEOS which contain 1% or less of low concentration ozone especially and an insulator layer is formed using the ozone content gas and TEOS containing 4% or more of high concentration ozone on the substrate insulator layer by which reforming was carried out, the compatibility on membrane formation with a substrate insulator layer and an insulator layer is very good, and is a desirable combination.

[Translation done.]

precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view (the 1) showing the manufacture approach of the semiconductor device concerning the substrate surface treatment approach of the gestalt operation of this invention.
[Drawing 2] It is the sectional view (the 2) showing the manufacture approach of the semiconductor device concerning the substrate surface treatment approach of the gestalt operation of this invention.
[Drawing 3] The thickness of Low O3/TEOS CVD SiO2 film concerning this example is received. It is the graph which shows the membrane formation velocity ratio of High O3/TEOS CVD SiO2 film.
[Drawing 4] It is the graph which shows the membrane formation velocity ratio to the plasma irradiation time concerning this example.
[Drawing 5] It is the sectional view showing the example which applied this invention to the trench slot concerning this example.
[Drawing 6] It is the sectional view showing the example which applied this invention between the metal wiring layers covered with plasma SiO2 film concerning this example.
[Drawing 7] It is the sectional view showing the example which applied this invention between the metal wiring layers which consist of wiring with which the quality of the materials concerning this example differ.
[Drawing 8] It is the sectional view showing the example which applied this invention between the metal lower layers which equipped the flank of wiring with the side all spacer concerning this example.
[Drawing 9] It is the side elevation showing the plasma equipment of the parallel monotonous mold of an anode plate coupling scheme used for plasma surface treatment processing of this example.
[Drawing 10] This example was started and membranes were formed. It is the photograph in which the condition of High O3/TEOS CVD SiO2 film is shown.
[Drawing 11] SiO2 film concerning a Prior art -- or -- Front-face top of Si3N4 film It is the sectional view showing the abnormality growth at the time of forming High O3/TEOS CVD SiO2 film.

[Drawing 12] It is the sectional view (the 1) showing the substrate surface treatment approach concerning a Prior art.
[Drawing 13] It is the sectional view (the 2) showing the substrate surface treatment approach concerning a Prior art.
[Drawing 14] It is the sectional view (the 3) showing the substrate surface treatment approach concerning a Prior art.
[Description of Notations]
1 Silicon Wafer (Substrate),
2 Wiring (Substrate),
3 Si3N4 Film (Substrate),
4 Six Slot (crevice),
5 Low O3/TEOS CVD SiO2 Film (Substrate Insulator Layer),
7 High O3/TEOS CVD SiO2 Film (Insulator Layer),
51 61 71 81 Silicon Wafer (Substrate),
52 Trench Slot (Crevice),

53, 62, 72, 82 SiO2 film (substrate),
54 Si3N4 Film (Substrate),
55, 65, 75, 85 Low O3/TEOS CVD SiO2 film (substrate insulator layer),
56, 67, 76, 87 High O3/TEOS CVD SiO2 Film (insulator layer),
63 73 Wiring (substrate),
64 Plasma SiO2 film (substrate),
66, 74, 86 Slot (crevice),
84 Sidewall spacer (substrate).

[Translation done.]

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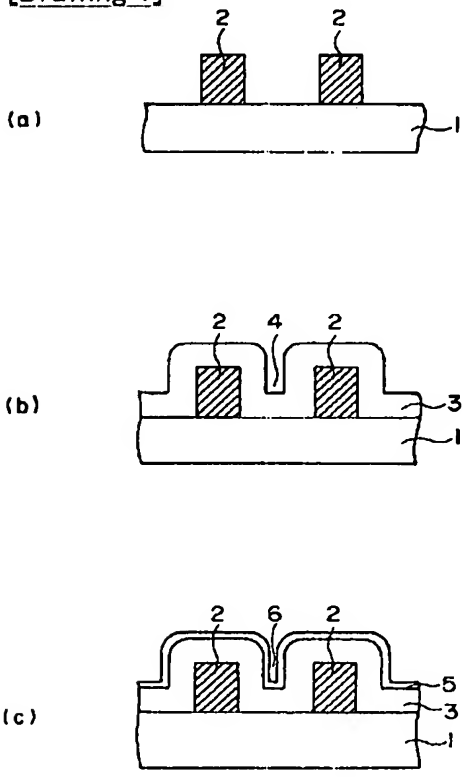
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

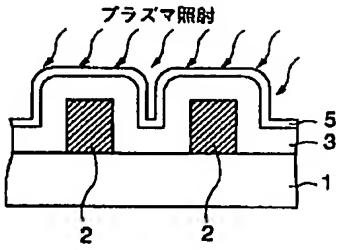
DRAWINGS

[Drawing 1]



[Drawing 2]

(a)



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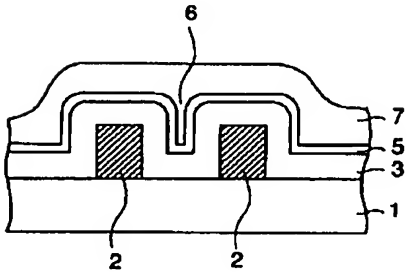
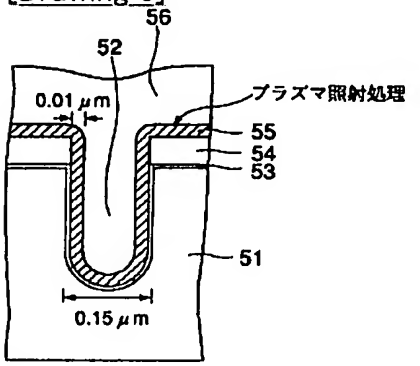
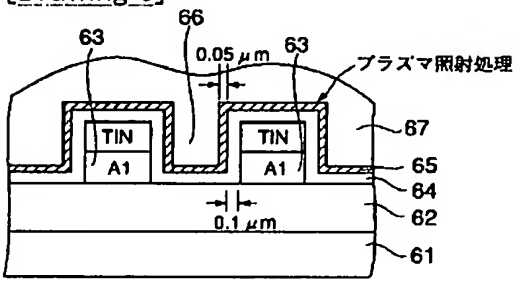


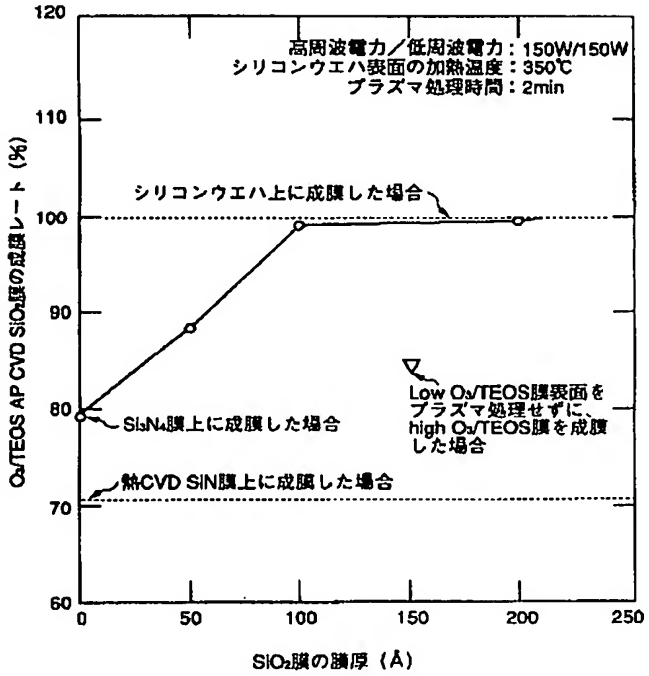
[Drawing 5]



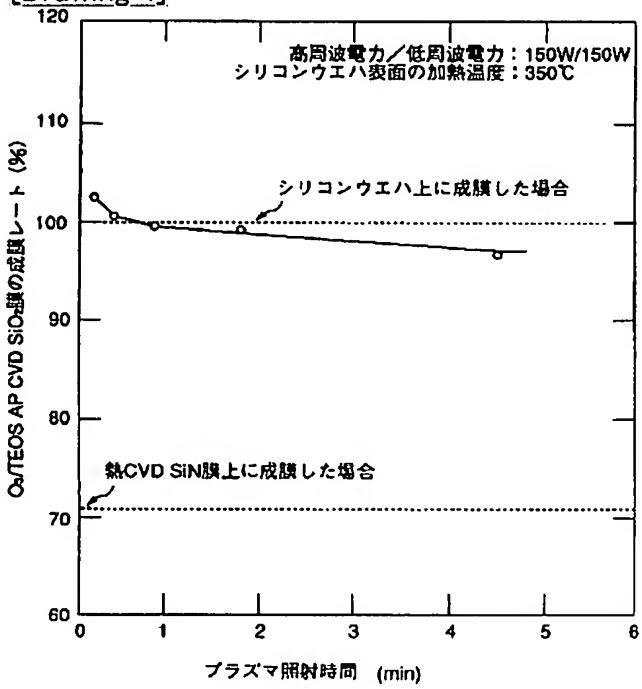
[Drawing 6]



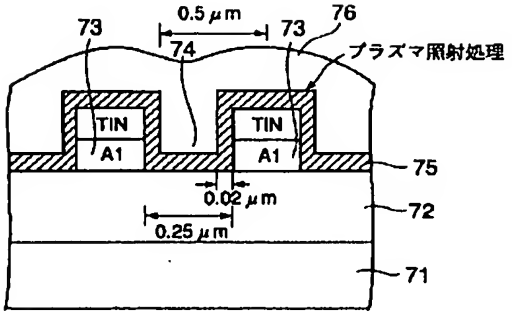
[Drawing 3]



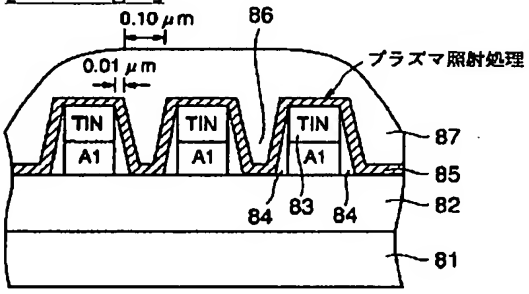
[Drawing 4]



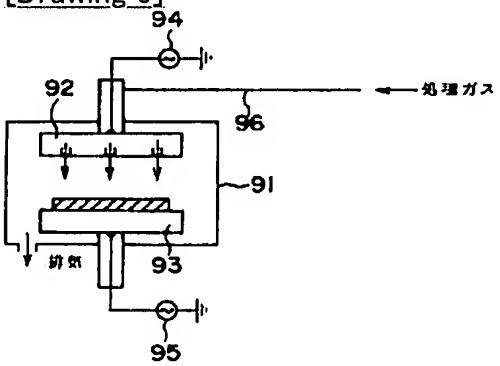
[Drawing 7]



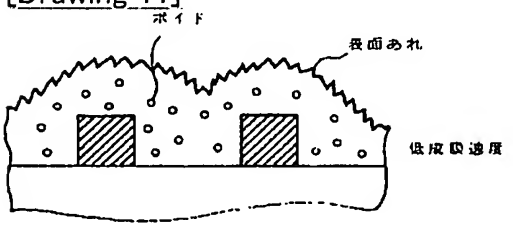
[Drawing 8]



[Drawing 9]



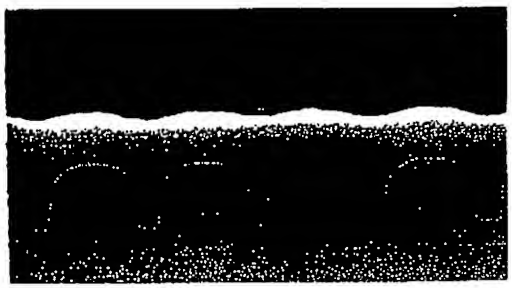
[Drawing 11]



[Drawing 10]

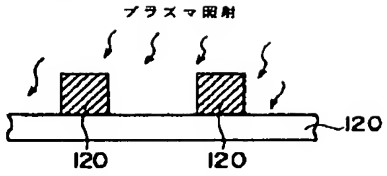
(a)

(b)

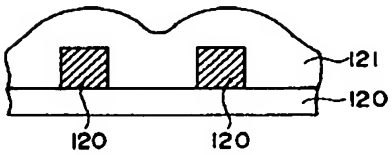


[Drawing 12]

(a)

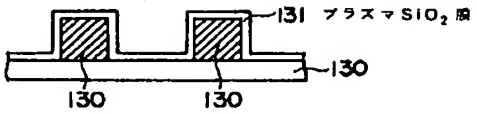


(b)



[Drawing 13]

(a)



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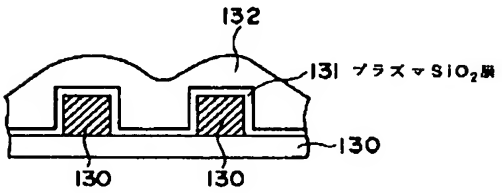
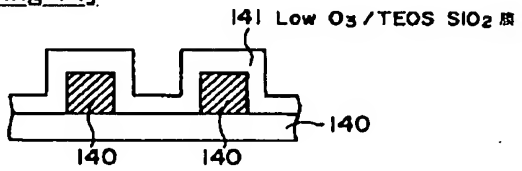


[Drawing 14]

(a)



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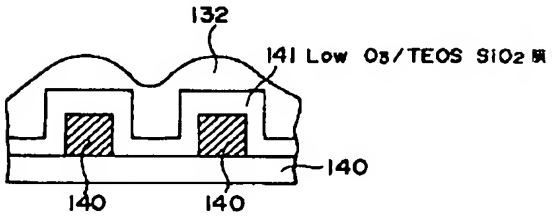

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WRITTEN AMENDMENT

---------- [a procedure revision]

[Filing Date] March 23, Heisei 11

[Procedure amendment 1]
[Document to be Amended] Specification
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[Proposed Amendment]
[Claim(s)]
[Claim 1] The substrate surface treatment approach characterized by forming 10nm or more of thickness, and a less than 100nm substrate insulator layer on a substrate, and putting and carrying out surface treatment of the front face of this substrate insulator layer to plasma gas before membrane formation.
[Claim 2] Said substrate is the substrate surface treatment approach according to claim 1 characterized by having a crevice field.
[Claim 3] Said crevice field is the substrate surface treatment approach according to claim 2 characterized by being the slot formed in said substrate, or being a crevice between the wiring layers formed on the insulating layer.
[Claim 4] The substrate surface treatment approach according to claim 1 to 3 characterized by silicon oxide or a silicon nitride being exposed to the front face of said substrate.
[Claim 5] Said substrate insulator layer is the substrate surface treatment approach according to claim 1 to 4 characterized by being either among silicon oxide, the PSG film, the BSG film, or the BPSG film.
[Claim 6] Said silicon oxide, the PSG film, the BSG film, or the BPSG film is the substrate surface treatment approach according to claim 5 characterized by making the mixed gas containing tetraethyl orthochromatic silicate and ozone content gas react, and forming.
[Claim 7] Said ozone content gas is the substrate surface treatment approach according to claim 6 characterized by the ozone levels in oxygen being 0.1% or more and 1% or less.
[Claim 8] Said silicon oxide is SiH2Cl2. N2O The substrate surface treatment approach according to claim 5 characterized by making it react and forming.
[Claim 9] Said silicon oxide is the substrate surface treatment approach according to claim 5 characterized by making tetraethyl orthochromatic silicate and oxygen react and forming.
[Claim 10] The substrate surface treatment approach according to claim 1 to 9 characterized by heating said substrate while having put the front face of said substrate insulator layer to plasma gas.

[Claim 11] The temperature of said substrate heating is the substrate surface treatment approach according to claim 10 characterized by being beyond a room temperature.
[Claim 12] The temperature of said substrate heating is the substrate surface treatment approach according to claim 11 characterized by being in the range of 100 degrees C or more and 400 degrees C or less.
[Claim 13] Said plasma gas is NH3, and helium, Ar and O2 at least. Or the substrate surface treatment approach according to claim 1 to 12 characterized by being generated using either among N2 O.
[Claim 14] The manufacture approach of the semiconductor device characterized by forming an insulator layer on said substrate insulator layer after performing reforming of a substrate insulator layer front face by the substrate surface treatment approach according to claim 1 to 13.
[Claim 15] Said insulator layer is the manufacture approach of the semiconductor device according to claim 14 characterized by being the silicon oxide which the ozone level in oxygen made the ozone content gas and tetraethyl orthochromatic silicate which are 4% or more react, and formed.
[Procedure amendment 2]
[Document to be Amended] Specification
[Item(s) to be Amended] 0011
[Method of Amendment] Modification

[Proposed Amendment]
[0011]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, invention according to claim 1 relates to the substrate surface treatment approach, forms 10nm or more of thickness, and a less than 100nm substrate insulator layer on a substrate before membrane formation, and is characterized by putting and carrying out surface treatment of the front face of this substrate insulator layer to plasma gas. Moreover, said substrate is characterized by having a crevice between a crevice field, for example, the slot formed in the substrate, or the wiring layer formed on the insulating layer.
[Procedure amendment 3]
[Document to be Amended] Specification
[Item(s) to be Amended] 0012
[Method of Amendment] Modification
[Proposed Amendment]
[0012] Moreover, said substrate insulator layer is characterized by being either among silicon oxide, the PSG film, the BSG film, or the BPSG film. These insulator layers make the mixed gas containing tetraethyl orthochromatic silicate and ozone content gas react, and are formed, and ozone content gas is characterized by the ozone levels in oxygen being 0.1% or more and 1% or less. Furthermore, said plasma gas is NH3, and helium, Ar and O2 at least. Or it is characterized by being generated using either among N2O.
[Procedure amendment 4]
[Document to be Amended] Specification
[Item(s) to be Amended] 0014
[Method of Amendment] Modification
[Proposed Amendment]
[0014] Below, an operation and effectiveness of this invention are explained. According to the substrate surface treatment approach of this invention, before membrane formation, 10nm or more of thickness and a less than 100nm substrate insulator layer are formed on a substrate, and surface treatment of the front face of this substrate insulator layer is put and carried out to plasma gas. Since the substrate insulator layer is formed on a substrate before membrane formation, the effect of the surface dependency of a substrate can be avoided without being based on the condition on the front face of a substrate. Furthermore, since the plasma exposure of the front face of a substrate insulator layer is carried out, the front face of a substrate insulator layer can be reformed. In this case, since what is necessary is just to reform the front face of the substrate insulator layer formed in the substrate front face instead of the front face itself of a substrate considered to have a different surface state for every form, the surface treatment approach communalized and standardized can be acquired.
[Procedure amendment 5]
[Document to be Amended] Specification
[Item(s) to be Amended] 0015
[Method of Amendment] Modification
[Proposed Amendment]
[0015] Since reforming of the front face of a substrate insulator layer is carried out by this when forming membranes on a substrate insulator layer, an insulator layer etc. can be formed on a substrate insulator layer, without being influenced of a substrate front face. Moreover, although there was a possibility of producing the abnormalities in membrane formation in response to the effect of a lower substrate front face in the pan of a substrate insulator layer since the thickness of a substrate insulator layer was thin when the thickness of a substrate insulator layer was less than 100nm and membranes were conventionally formed on the substrate insulator layer Since the plasma exposure of the front face of a substrate insulator layer was carried out, it turned out that

the membraneous quality of a substrate insulator layer becomes precise, and effect of the surface dependency of a substrate can be influenced and carried out even if it makes thickness of a substrate insulator layer thin.
[Procedure amendment 6]
[Document to be Amended] Specification
[Item(s) to be Amended] 0018
[Method of Amendment] Modification
[Proposed Amendment]
[0018] Furthermore, according to the manufacture approach of the semiconductor device of this invention, before membrane formation of an insulator layer, after forming 10nm or more of thickness, and a less than 100nm thin substrate insulator layer on a substrate, a substrate insulator layer front face is reformed and the insulator layer is formed on it by plasma exposure. For this reason, the good insulator layer of membraneous quality can be formed, without being able to apply also to the substrate which is the width of face about [of the thickness of a substrate insulator layer] Bai and which has a trench etc. (for example, between a trench slot and a metal wiring layer, between metal lower layers, etc.), and it is narrow, and being influenced of the surface dependency of a substrate.
[Procedure amendment 7]
[Document to be Amended] Specification
[Item(s) to be Amended] 0019
[Method of Amendment] Modification
[Proposed Amendment]
[0019] When a substrate insulator layer is formed using the ozone content gas and TEOS which contain 0.1 or more and 1% or less of low concentration ozone especially and an insulator layer is formed using the ozone content gas and TEOS containing 4% or more of high concentration ozone on the substrate insulator layer by which reforming was carried out, the compatibility on membrane formation with a substrate insulator layer and an insulator layer is very good, and is a desirable combination.
[Procedure amendment 8]
[Document to be Amended] Specification
[Item(s) to be Amended] 0054
[Method of Amendment] Modification
[Proposed Amendment]
[0054]
[Effect of the Invention] As mentioned above, according to the substrate surface treatment approach of this invention, before membrane formation, 10nm or more of thickness and a less than 100nm substrate insulator layer are formed on a substrate, further, a plasma exposure is carried out and surface treatment is carried out to the front face of a substrate insulator layer. Since the substrate insulator layer is formed on a substrate before membrane formation, the effect of the surface dependency of a substrate can be avoided without being based on the condition on the front face of a substrate.
[Procedure amendment 9]
[Document to be Amended] Specification
[Item(s) to be Amended] 0056
[Method of Amendment] Modification
[Proposed Amendment]
[0056] Moreover, the membraneous quality of a substrate insulator layer becomes precise, and even if it makes thickness of a substrate insulator layer thin with less than 100nm, it can avoid being influenced of the surface dependency of a substrate, since the plasma exposure is carried out on the front face of a substrate insulator layer. Therefore, formation of the substrate insulator layer to the substrate which has the crevice field of very narrow width of face is attained. When a substrate

insulator layer is formed on the substrate front face which has the crevice field of very narrow width of face using the ozone content gas and TEOS containing especially low concentration ozone, surface smoothness, step recovery ridge nature, and embedding nature are excellent, and, moreover, a substrate insulator layer with high compactness is obtained.

[Procedure amendment 10]
[Document to be Amended] Specification
[Item(s) to be Amended] 0057
[Method of Amendment] Modification
[Proposed Amendment]
[0057] Furthermore, according to the manufacture approach of the semiconductor device of this invention, before membrane formation of an insulator layer, after forming ten or more thickness and a less than 100nm substrate insulator layer on a substrate, a substrate insulator layer front face is reformed by plasma exposure, and the insulator layer is formed on it. For this reason, the good insulator layer of membraneous quality can be formed, without [minutely and] being able to apply also to the substrate which has a trench etc. and being influenced of the surface dependency of a substrate. When an insulator layer is formed using the ozone content gas and TEOS containing 4% or more of high concentration ozone on the substrate insulator layer by which reforming was carried out after forming and reforming a substrate insulator layer using the ozone content gas and TEOS which contain 0.1 – 1% of low concentration ozone especially, the compatibility on membrane formation with a substrate insulator layer and an insulator layer is very good, and is a desirable combination.

[Translation done.]